CLAIMS

What is claimed is:

1. A semiconductor wafer comprising:

a plurality of fields on the wafer; and

a plurality of alignment fields within the plurality of fields, each alignment field having a plurality of intra-field overlay alignment mark pairs therearound for in-situ, non-passive intra-field alignment correction.

2. The semiconductor wafer of claim 1, wherein the plurality of fields comprises the plurality of alignment fields correspond to semiconductor dies.

3. The semiconductor wafer of claim 1, wherein the plurality of fields comprises the plurality of alignment fields correspond to semiconductor devices.

4. The semiconductor wafer of claim 1, wherein the plurality of intra-field overlay alignment mark pairs numbers between two and four.

5. The semiconductor wafer of claim 1, wherein each of the plurality of intra-field overlay alignment mark pairs comprises a pair of extra scribe-lane marks.

6. The method comprising:

providing a semiconductor wafer;

defining a plurality of fields on the semiconductor wafer, including a plurality of alignment fields; and,

providing a plurality of intra-field overlay alignment mark pairs around each of the plurality of alignment fields to provide for non-passive intra-field alignment correction.

7. The method of claim 6, wherein providing the plurality of fields comprises providing a plurality of fields corresponding to semiconductor dies.

8. The method of claim 6, wherein providing the plurality of fields comprises providing a plurality of fields corresponding to semiconductor devices.

9. The method of claim 6, wherein providing the plurality of fields comprises providing between two and four of the plurality of alignment intra-fields.

10. The method of claim 6, wherein providing the plurality of intra-field overlay alignment mark pairs around each of the plurality of alignment fields comprises providing between two and four of the plurality of overlay alignment mark pairs around each of the plurality of alignment fields.

11. The method of claim 6, wherein providing the plurality of intra-field overlay alignment mark pairs around each of the plurality of alignment fields comprises providing a plurality of extra scribe-lane mark pairs around each of the plurality of alignment fields.

12. A semiconductor wafer comprising:

a plurality of fields;

a pair of alignment fields within the plurality of fields, further comprising an alignment field having 2-4 pairs of intra-field overlay alignment mark pairs there around for in-situ, non-passive intra-field alignment correction.

13. The semiconductor wafer of claim 12, wherein the plurality of fields comprising the pair of alignment fields correspond to semiconductor dies.

14. The semiconductor wafer of claim 12, wherein the plurality of fields comprising the pair of alignment fields correspond to semiconductor devices.

15. The semiconductor wafer of claim 12, wherein each of the pair of intra-field overlay alignment mark pairs comprises a pair of extra scribe-lane marks.